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| 10/813,003 | 03/31/2004 | Jerry Chow | 77682-230 /aba | 5213 |

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| EXAMINER | |
|---|---|
| KIM, JUNG W | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/813,003 | CHOW, JERRY | |
| | Examiner | Art Unit | |
| | Jung Kim | 2132 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *see enclosed*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-40 are pending.

### *Information Disclosure Statement*

2. The IDS submitted on 1/5/05 has been considered. An initial copy is enclosed.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 4, 7-19, 21-27, 29-33 and 35-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Beukema et al. US Patent Application Publication No. 20020124148 (hereinafter Beukema).

5. As per claims 1, 2, 4, 7-15, Beukema discloses a memory protection system comprising:

a. a key store storing identifiers of protected memory locations and respective corresponding memory protection keys; and a memory access

manager configured to receive a memory command for altering contents of any of the protected memory locations, and for each memory command, to determine whether the memory command includes a memory protection key corresponding to at least one of said protected memory locations to be altered, and, where the memory command includes the memory protection key corresponding to each protected memory location to be altered, to permit the memory command and then render each memory protection key in the command inaccessible (paragraph 54; by virtue of de-allocating memory; see also applicant's specification, pg. 17, lines 19-26);

b. wherein the identifiers comprise addresses in a protected memory; wherein the identifiers identify data entries in a protected memory; (paragraph 54; pointer to an associated memory region/address)

c. wherein the key store stores a mapping table that maps each identifier to a corresponding memory protection key; (paragraph 54; "Protection/Translation Table");

d. wherein at least one of the identifiers is mapped to multiple corresponding memory protection keys (paragraph 54; L_key and R_key);

e. the system implemented in an electronic device having a memory, the memory comprising the protected memory locations and unprotected memory locations (paragraph 55, and fig. 6);

f. wherein the memory access manager is further configured to receive memory commands for altering contents of the unprotected memory locations,

and to permit the memory commands for altering contents of the unprotected memory locations and each memory command for altering contents of any protected memory location that includes the memory protection key corresponding to each protected memory location to be altered. (paragraph 59; fig. 7)

g. wherein the memory access manager is further configured to perform each memory command that includes the memory protection key corresponding to each protected memory location to be altered (paragraphs 54 and 59);

h. the system implemented in an electronic device, wherein the memory commands are received by the memory access manager from an originating electronic device component, and wherein the originating electronic device component proceeds with each memory command permitted by the memory access manager; wherein the originating electronic device component is a memory update module; wherein the originating electronic device component sends memory commands to the memory access manager responsive to data received at the electronic device; wherein the originating electronic device component is further configured to extract a received memory protection key from the received data and to provide the received memory protection key to the memory access manager. (fig. 2; paragraphs 54-56; external user supplies protection key for rights access (read, write) to protected memory)

6. As per claims 16-19 and 21, Beukema discloses an electronic device comprising:

i. a memory; a receiver configured to receive data to be written to the memory; and a memory protection system associating protected memory locations in the memory with respective corresponding keys, and configured to allow the received data to be written to any of the protected memory locations only if the received data includes a key corresponding to the protected memory location to which the received data is to be written and to render the corresponding key in the received data inaccessible after allowing the received data to be written to the protected memory location (figs. 6 and 7; paragraphs 53 and 54);

j. wherein the memory comprises unprotected memory locations into which the received data is written (paragraph 55, and fig. 6);

k. wherein each key is rendered inaccessible by erasing the received data from the unprotected memory locations where the memory access manager allows the received data to be written to the protected memory locations (by virtue of de-allocating memory; see also applicant's specification, pg. 17, lines 19-26);

l. wherein the memory protection system comprises: a key store storing a mapping table that associates the protected memory locations with the respective corresponding keys; and a memory access manager configured to process memory a command for writing the received data to any of the protected memory locations, to determine whether the received data includes the key corresponding to any of the protected memory locations to which the received

data is to be written, and, where the received data includes the key corresponding to a protected memory location to which the received data is to be written, to permit the memory command and then render the corresponding key in the received data inaccessible (paragraph 54);

m. wherein the receiver comprises one or more components selected from the group consisting of: a wireless receiver, a wireless transceiver, a modem, a network interface, a serial port, a parallel port, a Universal Serial Bus (USB) port, an infrared port, and a short-range wireless communication module. (Fig. 1, reference no. 100)

7. As per claims 22-27 and 29-33, Beukema discloses a method of protecting memory in an electronic device, comprising:

n. receiving a memory command to alter a protected memory location; identifying a memory protection key corresponding to the protected memory location; determining whether the memory command includes the memory protection key corresponding to the protected memory location; permitting completion of the memory command where the memory command includes the memory protection key corresponding to the protected memory location (paragraphs 53-59); and rendering the memory protection key in the memory command inaccessible (by virtue of de-allocating memory; see also applicant's specification, pg. 17, lines 19-26);

o. wherein permitting comprises performing the memory command (paragraphs 54 and 59);

p. wherein receiving comprises receiving the memory command from an originating electronic device component, and wherein permitting comprises allowing the originating electronic device component to perform the memory command; (paragraph 55, and fig. 6)

q. receiving data to be written to the protected memory location; and generating the memory command responsive to receiving the data (paragraph 54, request is a write access request);

r. wherein the received data comprises a received key, and wherein generating comprises extracting the received key from the received data and inserting the received key into the memory command (paragraph 57);

s. wherein determining comprises comparing the memory protection key corresponding to the protected memory location with the received key in the memory command (paragraphs 54 and 59);

t. further comprising the step of: storing the received data to an unprotected memory location, wherein rendering the memory protection key in the memory command inaccessible comprises erasing the received data from the unprotected memory location upon completion of the memory command; (by virtue of de-allocating memory; see also applicant's specification, pg. 17, lines 19-26)

u. wherein identifying comprises identifying a protected memory location in the memory command and accessing a mapping table that maps protected

memory locations to respective corresponding memory protection keys (paragraph 54);

v. wherein the memory command comprises one of a memory write command and a memory erase command (paragraphs 54 and 59);

w. further comprising: receiving memory commands to alter unprotected memory locations; and permitting completion of the memory commands to alter unprotected memory locations (paragraphs 54 and 59);

x. further comprising: receiving memory read commands; and permitting completion of the memory read commands. (paragraphs 54 and 59)

8. As per claim 35, Beukema further discloses a computer-readable medium storing instructions for performing the method of claim 22. (paragraph 60)

9. As per claims 36-40, Beukema discloses a method of protecting electronic memory, comprising:

y. configuring a memory store of an electronic device into at least one protected memory location and a key store operable to store an identifier of each protected memory location and a respective corresponding memory protection key; and configuring a processor of the electronic device to provide a memory access manager operable to receive memory commands for altering contents of any of the at least one protected memory location, and for at least one memory command, to determine whether the memory command includes a memory

protection key corresponding to at least one protected memory location to be modified, said memory command including the memory protection key corresponding to at least one said protected memory location to be modified, to permit the memory command and then render each corresponding memory protection key in the command inaccessible; (paragraphs 53-59)

z. wherein the memory store comprises the protected memory locations and unprotected memory locations (paragraph 55; fig. 6);

aa. wherein configuring the processor comprises installing memory access manager software on the electronic device for execution by the processor. (paragraph 60)

10. As per claims 39 and 40, Beukema further discloses a computer-readable medium storing instructions for performing the method of claims 36 and 38, and the memory access manager software. (paragraph 60)

11. Claims 1, 3-6, 22 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by England et al. USPN 7,194,092 (hereinafter England).

12. As per claims 1 and 3-6, England discloses a memory protection system comprising:

bb. a key store storing identifiers of protected memory locations and respective corresponding memory protection keys; and a memory access

manager configured to receive a memory command for altering contents of any of the protected memory locations, and for each memory command, to determine whether the memory command includes a memory protection key corresponding to at least one of said protected memory locations to be altered, and, where the memory command includes the memory protection key corresponding to each protected memory location to be altered, to permit the memory command and then render each memory protection key in the command inaccessible (col. 10:41-51; by virtue of de-allocating memory; see also applicant's specification, pg. 17, lines 19-26);

cc. wherein the identifiers comprise names of protected files in a memory; wherein the identifiers identify data entries in a protected memory; (10:31-35; 16:33-37).

dd. wherein each of the memory protection keys comprises a modified version of a data sequence; wherein the modified version comprises a hash of the data sequence. (10:41-51; 17:1-30; 17:57-18:14)

13. As per claims 22 and 34, England discloses a method of protecting memory in an electronic device, comprising:

ee. receiving a memory command to alter a protected memory location; identifying a memory protection key corresponding to the protected memory location; determining whether the memory command includes the memory protection key corresponding to the protected memory location; permitting

completion of the memory command where the memory command includes the memory protection key corresponding to the protected memory location; and rendering the memory protection key in the memory command inaccessible; (col. 10:41-51)

ff. wherein said identifying step comprises accessing the memory protection key corresponding to the protected memory location in a key store, the method further comprising: receiving a command to establish a new protected memory location in the memory and a memory protection key corresponding to the new protected memory location; establishing the new protected memory location in the memory; and storing the memory protection key in the key store. (10:14-40)

***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 20 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beukema.

16. As per claim 20, the rejection of claim 19 under 35 USC 102(e) as being anticipated by Beukema is incorporated herein. Beukema further discloses the key store resides at a secure location in the memory separate from the remainder of the

memory. (paragraph 54) Although Beukema does not expressly disclose the remainder of the memory is a filesystem, it is notoriously well known in the art for SANs to provide storage access to a filesystem, to enable multiple computers access to the filesystem. Official Notice of this teaching is taken. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made for the memory to comprise a file system, and wherein the key store resides at a secure location in the memory outside of the file system, since a file system provides ease of storing and organizing computer data as known to one of ordinary skill in the art. The aforementioned cover the limitations of claim 20.

17. As per claim 28, the rejection of claim 26 under 35 USC 102(e) as being anticipated by Beukema is incorporated herein. Beukema does not expressly disclose wherein determining comprises retrieving a modified version of the memory protection key corresponding to the protected memory location, modifying the received key in the memory command to generate a modified received key, and comparing the modified received key to the modified version of the memory protection key corresponding to the protected memory location; however, it is notoriously well known in the art to use and store a hash value of an identifier as opposed to the original identifier. A hash value uniquely maps an original value to a modified value, such that the modified value is typically much smaller than the original value. Hence, the modified value retains the unique property of the original value but requires less memory and bandwidth requirements to store and communicate the value. Therefore, it would be obvious to

one of ordinary skill in the art at the time the invention was made wherein the determining step comprises retrieving a modified version of the memory protection key corresponding to the protected memory location, modifying the received key in the memory command to generate a modified received key, and comparing the modified received key to the modified version of the memory protection key corresponding to the protected memory location. One would be motivated to do so to preserve memory and processing resources as known to one of ordinary skill in the art. The aforementioned cover the limitations of claim 28.

***Communications Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung W. Kim whose telephone number is 571-272-3804. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jung W Kim
Examiner
Art Unit 2132